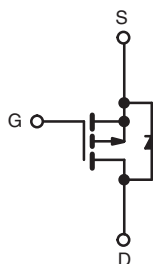
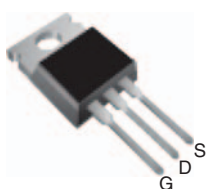


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	1.5
Q_g (Max.) (nC)	22	
Q_{gs} (nC)	12	
Q_{gd} (nC)	10	
Configuration	Single	

TO-220


P-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available


RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRF9620PbF
	SiHF9620-E3
SnPb	IRF9620
	SiHF9620

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	- 3.5	A
		$T_C = 100\text{ }^{\circ}\text{C}$		- 2.0	
Pulsed Drain Current ^a			I_{DM}	- 14	
Linear Derating Factor				0.32	W/ $^{\circ}\text{C}$
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		P_D	40	W
Peak Diode Recovery dV/dt^b			dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 $^{\circ}$	
Mounting Torque	6-32 or M3 screw			10	
				1.1	N · m

Notes



- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $I_{SD} \leq -3.5$ A, $dI/dt \leq 95$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

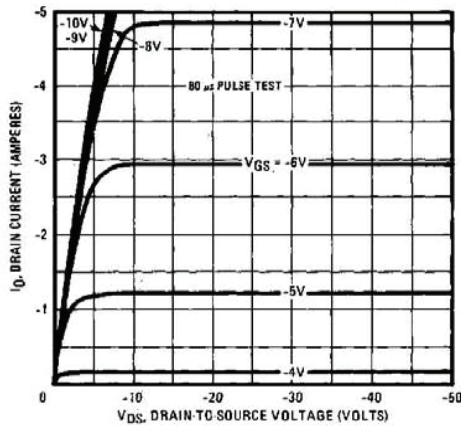
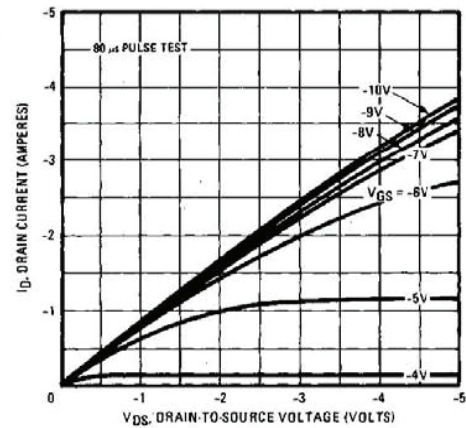
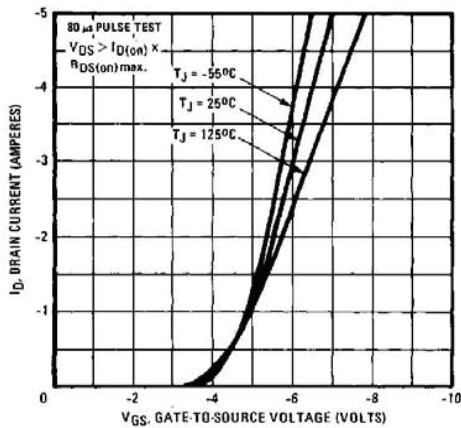
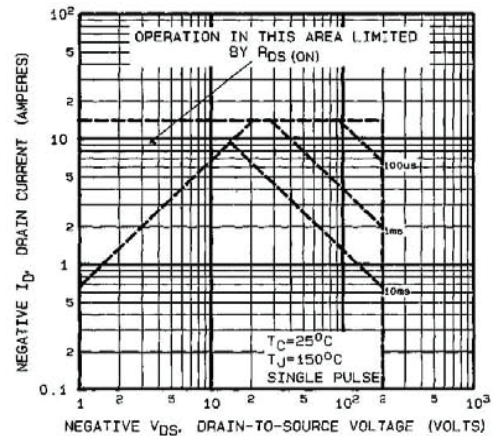
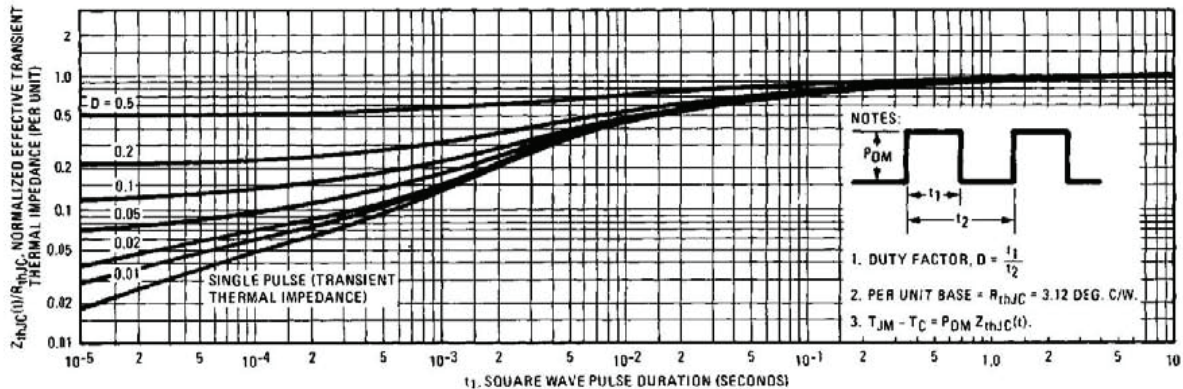
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = - 1 mA		-	- 0.22	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 200 V, V _{GS} = 0 V		-	-	- 100	μA
		V _{DS} = - 160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	- 500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 1.5 A ^b	-	-	1.5	Ω
Forward Transconductance	g _{fs}	V _{DS} = - 50 V, I _D = - 1.5 A ^b		1.0	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	350	-	pF
Output Capacitance	C _{oss}			-	100	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 4.0 A, V _{DS} = - 160 V, see fig. 11 and 18 ^b	-	-	22	nC
Gate-Source Charge	Q _{gs}			-	-	12	
Gate-Drain Charge	Q _{gd}			-	-	10	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 100 V, I _D = - 1.5 A, R _G = 50 Ω, R _D = 67 Ω, see fig. 17 ^b		-	15	-	ns
Rise Time	t _r			-	25	-	
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Fall Time	t _f			-	15	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 3.5	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 14	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 3.5 A, V _{GS} = 0 V ^b		-	-	- 7.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 3.5 A, dI/dt = 100 A/μs ^b		-	300	450	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.9	2.9	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Saturation Characteristics

Fig. 2 - Typical Transfer Characteristics

Fig. 4 - Maximum Safe Operating Area

Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

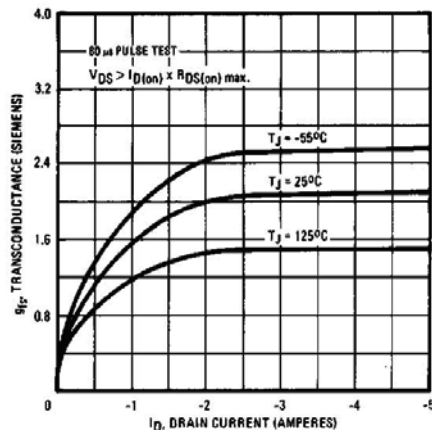


Fig. 6 - Typical Transconductance vs. Drain Current

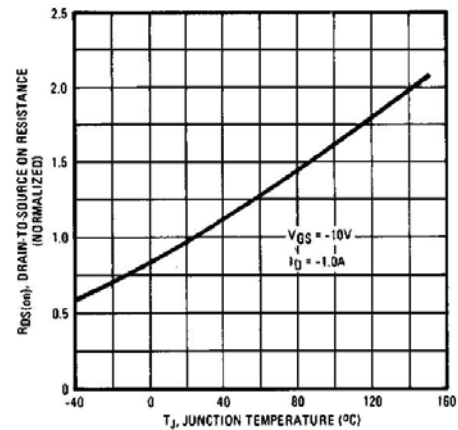


Fig. 9 - Normalized On-Resistance vs. Temperature

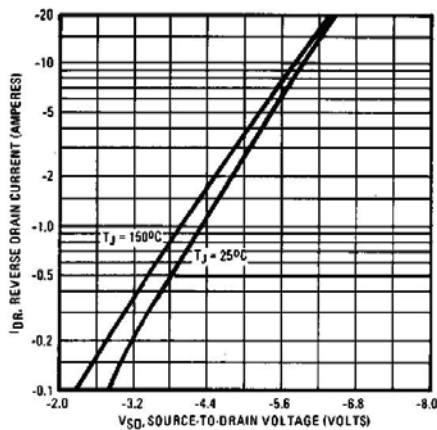


Fig. 7 - Typical Source-Drain Diode Forward Voltage

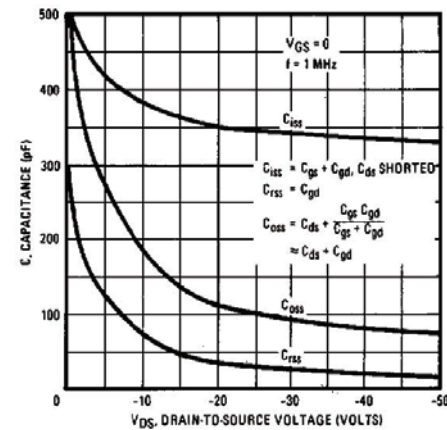


Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

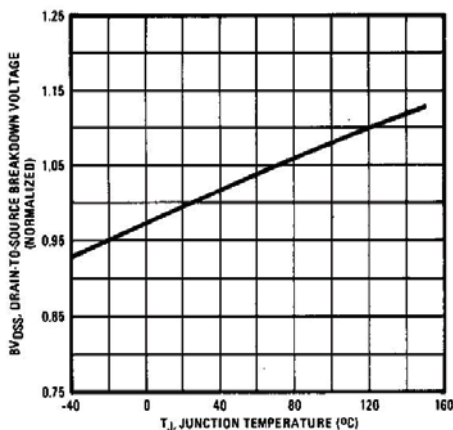


Fig. 8 - Breakdown Voltage vs. Temperature

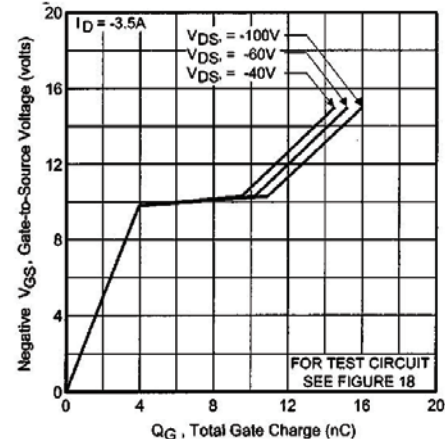


Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

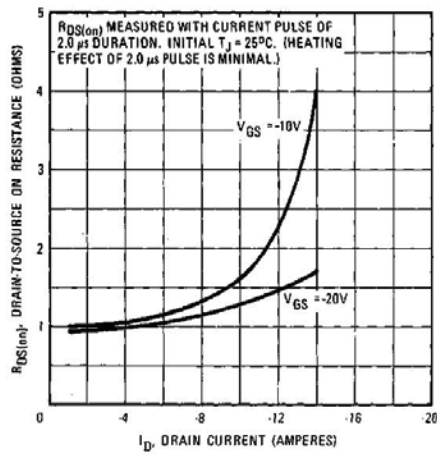


Fig. 12 - Typical On-Resistance vs. Drain Current

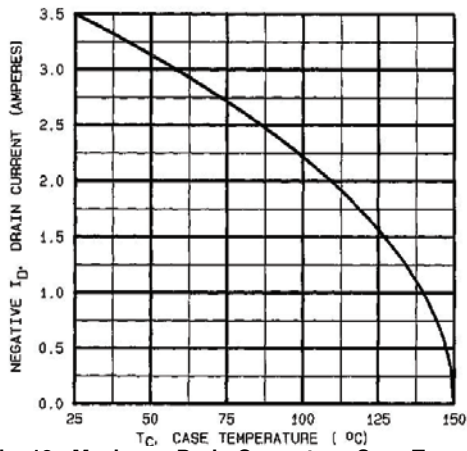


Fig. 13 - Maximum Drain Current vs. Case Temperature

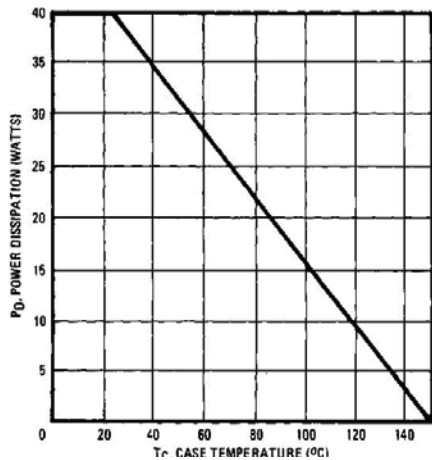


Fig. 14 - Power vs. Temperature Derating Curve

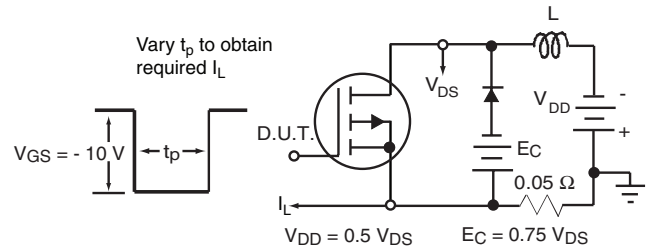


Fig. 15 - Clamped Inductive Test Circuit

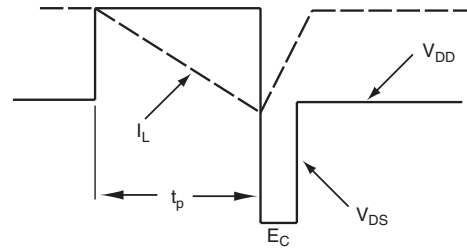


Fig. 16 - Clamped Inductive Waveforms

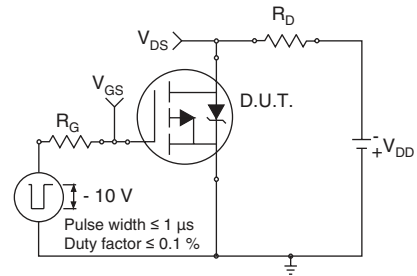


Fig. 17a - Switching Time Test Circuit

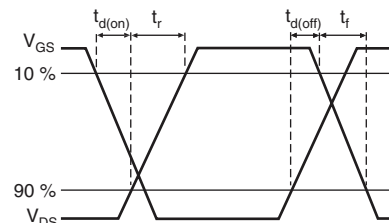


Fig. 17b - Switching Time Waveforms

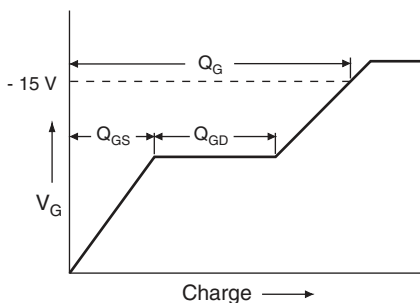


Fig. 18a - Basic Gate Charge Waveform

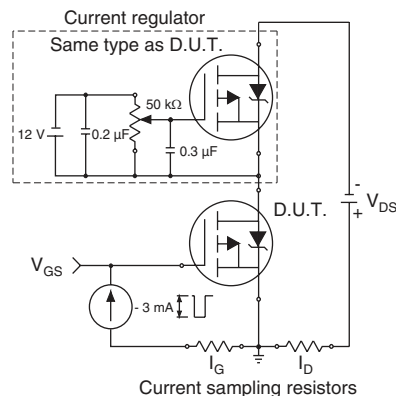
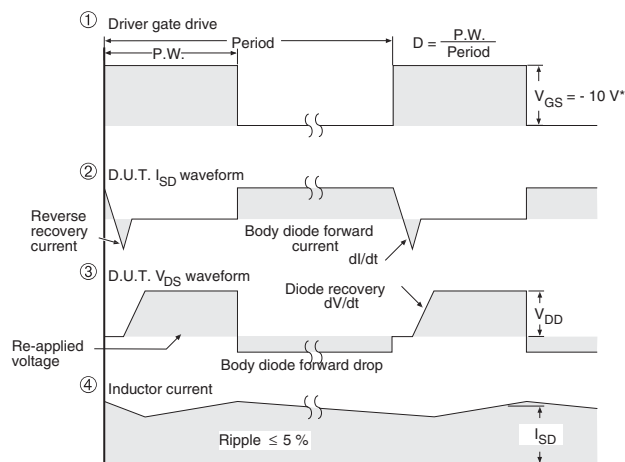
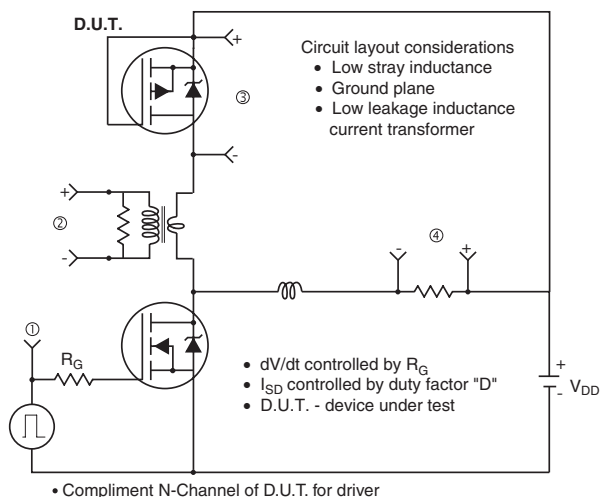


Fig. 18b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5$ V for logic level and -3 V drive devices

Fig. 19 - For P-Channel

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